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Reg. No. : .....

Name : .....

Sixth Semester B.Tech. Degree Examination, May 2016
(2013 Scheme)
13.602 : VLSI DESIGN (T)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all**, **each** carries **2** marks :

1. Compare electron beam and photo lithography.
2. Define Fick's diffusion laws.
3. Define threshold voltage. How it can be controlled ?
4. What are the properties of the metal used for metallization ?
5. What are the undesirable capacitances formed in MOS fabrication ?
6. Define the noise margin for CMOS inverter.
7. Define equations for static and dynamic power dissipation.
8. Why the pseudo NMOS is ratioed ?
9. Draw the basic FPGA structure.
10. Draw a DRAM memory cell. **(2×10=20 Marks)**

PART – B

Answer **any one** question from **each Module** :

Module – 1

11. a) With diagram explain the CZ process of crystal growth. 10

    b) Assuming Gaussian distribution for the ion implantation, find the distance from the surface at which the ion concentration falls to half the peak value, for a range of 0.1 μ. The straggle value is 0.02 μ. 6

    c) What is the shift in threshold voltage for $\phi_b = 0.375$ and $\gamma = 0.57$. Let $V_{SB} = 2.5V$. 4

OR

12. a) With neat sketch, explain the CVD process. 10

    b) Explain different diffusion profiles with relevant equations. 10

Module – 2

13. a) Explain the twin-tub process flow for CMOS fabrication. 10

    b) Derive the $I_D - V_{DS}$ relationship in a MOSFET. 10

OR

14. a) Explain the short channel effects in MOSFET. 10

    b) Derive the expression for MOSFET threshold voltage. 10

Module – 3

15. a) Derive expression for switching threshold of a CMOS inverter. 10

    b) Design a pass transistor logic for 2 input XNOR gate. 4

    c) What are the advantages and disadvantages of domino logic ? 6

OR

16. a) Derive graphically, the CMOS inverter characteristics. 10

    b) Show the design of a 32 bit carry select adder based on 4 bit or similar ripple carry adder. Find the total gate delay for your design. 10

Module – 4

17. a) Design and AND-OR PLA, with outputs,

    $F1 = m_1 + m_6$

    $F2 = m_0 + m_5 + m_6 + m_7$

    $F3 = m_3 + m_4 + m_7$. 10

    b) What is the purpose of sense amplifier ? Explain any one type. 10

OR

18. a) Draw a ROM array to store a set of Eight, 8-bit data using MOS based ROM. Explain how they are written and read ? 10

    b) Explain the system level VLSI test techniques. 10